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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,037	06/19/2003	Hannu Huotari	ASMMC.047AUS	8258

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EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,037	HUOTARI, HANNU	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-24 and 27-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-24 and 27-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed November 8, 2004.

Response to Amendment

The amendment filed November 8, 2004 has been entered and made of record.

Information Disclosure Statement

The information disclosure statement filed November 8, 2004 fails to comply with 37 CFR 1.97(d) because it lacks a statement as specified in 37 CFR 1.97(e). It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 15-24, 27-38 and 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (US 6,166,417, previously cited) in view of Elers et al. (WO 01/29893 A1, previously cited) and Pomarede et al. (US 6,613,695, previously cited).

Regarding claim 1, Bai discloses depositing a gate dielectric layer (120) over first and second regions (105/115) of a substrate, depositing a barrier layer (125) directly over the gate dielectric layer such that it overlies both the first and second regions, and forming first and second gate electrode layers (130/135) over the first -and second regions, respectively (col. 3, ln. 17 - col. 4, ln. 64). Bai states that the function of the barrier layer is to "inhibit interaction between the gate dielectric and the gate electrode." Thus, the barrier layer must be able to keep metal atoms in the gate electrode from diffusing into the underlying gate dielectric.

Bai does not disclose by what method the barrier layer may be deposited. Like Bai, Elers discloses depositing a barrier layer onto a layer of SiO_2 dielectric. Elers states that it is advantageous to form barrier layers such that they are nanolaminates because nanolaminates "have enhanced diffusion barrier properties" by virtue of their structure having "very complicated diffusion paths for impurities through disruption of normal crystal growth during deposition" (pg. 8, ln. 20-25). The nanolaminate barrier layer is formed by an ALD (atomic layer deposition process) (pg. 1, ln. 28-32). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the barrier layer of Bai such that it is a nanolaminate deposited by ALD because Elers teaches that a nanolaminate structure provides enhanced diffusion barrier properties and Elers teaches that ALD is the way in which such a structure is created.

Bai discloses that the gate dielectric layer may be grown or deposited. Bai also states that the gate dielectric may be a high dielectric constant (high-k) layer (col. 3, ln. 17-26). However, Bai does not disclose that the gate dielectric layer is deposited by an ALD process. Like Bai, Pomarede discloses depositing a high-k gate dielectric layer on a semiconductor substrate. Pomarede teaches that the high-k gate dielectric layer can be advantageously deposited by using an ALD process. Pomarede teaches that the ALD process is self-limiting and can be used to precisely control the thickness of the gate dielectric layer since the process deposits only one monolayer of atoms at a time (col. 11, ln. 13 – col. 12, ln. 67). At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit the high-k gate dielectric layer of Bai by using the ALD process because Pomarede teaches that it is advantageous to

deposit a high-k gate dielectric layer using ALD in order that the thickness of the gate dielectric layer may be controlled precisely.

Regarding claim 16, Bai discloses that one of the regions is a PMOS region and the other region is an NMOS region (col. 3, ln. 8-16).

Regarding claim 17, Bai discloses the first and second gate electrode layers are adjacent (Fig. 7).

Regarding claim 18, Bai discloses that the first gate electrode layer includes a first gate electrode material and the second gate electrode includes a second gate electrode material (col. 3, ln. 55-65; col. 4, ln. 41-53).

Regarding claims 19 and 20, Bai discloses that if the first gate electrode is made of N-type material, the second electrode will be made of P-type material, and vice-versa. The first gate electrode material may include nickel or ruthenium oxide if the material is to have the work function of a P-type doped semiconductor or may include ruthenium if the material is to have the work function of an N-type doped semiconductor. The same is true for the second gate electrode. Hence, the first and second gate electrodes will be made of different conductive materials. See col. 1, ln. 42-54; col. 3, ln. 55 – col. 4, ln. 9; col. 4, ln. 41-53).

Regarding claim 21, Bai discloses that the first and second gate electrode materials may be made of nickel, ruthenium oxide or ruthenium (col. 1, ln. 41-53; col. 4, ln. 3-9; col. 4, ln. 42-53).

Regarding claim 22, Bai discloses that one of the gate electrodes may be made of a metal nitride (MoN) (col. 1, ln. 41-53).

Regarding claims 23 and 24, Bai discloses that the barrier layer may be TiN or TaN, both of which are conductive material (col. 3, ln. 51-54).

Regarding claims 27 and 28, Bai discloses that the barrier layer has a thickness of 5 – 200 (col. 3, ln. 36-37).

Regarding claims 29-32, Bai discloses that the gate dielectric layer may be a high-k layer, but Bai does not disclose a method of forming the dielectric layer, nor treating the dielectric layer to remove OH groups. Pomarede teaches that it is advantageous to treat a layer such as a high-k gate dielectric layer with a mixture including ammonia (nitrogen-hydrogen) plasma and nitrogen radicals upon which subsequent layers will be deposited (col. 13, ln. 1 – col. 14, ln. 17). This process inherently replaces OH groups on the surface of the high-k dielectric layer with nitrogen atoms. Pomarede states, "By changing the surface termination of the substrate [high-k dielectric] with a low temperature radical treatment, subsequent deposition is advantageously facilitated without significantly affecting the bulk properties of the underlying material." (Abstract). At the time of the invention, it would have been obvious to one of ordinary skill in the art to treat the surface of the gate dielectric film of Bai as is taught by Pomarede because Pomarede teaches that it is advantageous to change the surface termination of a high-k gate dielectric film that will have additional layers subsequently deposited thereon.

Regarding claim 33, Bai discloses depositing a layer of first gate electrode material (130 or 135 can be considered "a first gate electrode layer") over the first and second regions of the substrate (Fig. 4 and 6).

Regarding claim 34, Bai discloses removing the first gate electrode material from over the second region without removing the underlying barrier layer (Fig. 5 and 7).

Regarding claim 35, in the event that the material 135 is considered to be the first gate electrode material, Bai discloses that the first gate electrode material is removed from over the second region by chemical mechanical polishing (col. 4, ln. 55-64).

Regarding claim 36, Bai discloses depositing a layer of second gate electrode material (130 or 135 can be considered "a second gate electrode layer") over the first and second regions of the substrate (Fig. 4 and 6).

Regarding claim 37, in the even that the material 130 is considered to be the first gate electrode material, Bai discloses that the first gate electrode material is removed from over the second region by differential etching (col. 29-33).

Regarding claims 38 and 41, Bai discloses depositing a layer of second gate electrode material (130 or 135 can be considered "a second gate electrode layer") over the first and second regions of the substrate and removing the second gate electrode material from over the first region without removing the underlying barrier layer (Fig. 5, 7 and 8).

Regarding claim 40, Bai discloses etching the barrier layer over portions of the second region to a thickness of 0 Angstroms (Fig. 8).

Regarding claim 42, Bai discloses depositing a dielectric layer (120) over first and second regions (105/115) of a substrate, depositing a barrier layer (125) directly over the dielectric layer such that it overlies both the first and second regions, depositing a first gate electrode material (130 or 135) over the first and second regions, removing the first gate electrode material from over the first region without removing the barrier layer, depositing a second gate electrode material (135 or 130), and defining a first and second electrode in the first and second regions.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. (US 6,166,417) in view of Elers et al. (WO 01/29893 A1) and Pomarede et al. (US 6,613,695), as applied to claim 15 above, and further in view of Chang et al. (US 6,660,630, previously cited).

Regarding claim 39, Bai does not disclose depositing a layer of conductive material over the first and second gate electrode layers. However, as is disclosed by Chang, it is necessary in the fabrication of semiconductor devices such as that of Bai, to deposit multi-layered conductive interconnection structures above the gates of a semiconductor device in order to provide required wiring to the gates of the device (col. 1, ln. 34-65). Such structures are well-known in the art. At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit conductive material over the first and second gate electrode layers of Bai for the purpose of forming a multi-layered interconnection structure that connects the gate with upper-level wiring because such structures are necessary to the function of the gate and are well-known in the art.

Response to Arguments

Applicant's arguments filed November 8, 2004 have been fully considered.

The Examiner agrees with Applicant's argument that neither Bai nor Elers teach the limitation recited in claim 15 of depositing the underlying dielectric layer by an atomic layer deposition process. Therefore, the Pomarede reference has been added to the rejection of claim 15, as it teaches using ALD to deposit a gate dielectric layer.

Regarding claims 15 and 42, Applicant argues that Elers allegedly fails to provide motivation for forming the barrier layer of Bai such that it is an ALD nanolaminate because Elers' barrier layer is used in a damascene structure, whereas Bai's barrier layer is used in a gate

electrode. The motivation for combining the teachings of Elers with the invention of Bai is that Bai teaches no method of forming the barrier layer, while Elers teaches that the specific method of forming a barrier layer such that it is a nanolaminate deposited by ALD serves to form an unusually successful barrier layer because such a layer has "very complicated diffusion paths for impurities through disruption of normal crystal growth during deposition". Elers teaches that, in particular, this barrier layer can be used to prevent diffusion between an overlying metal layer and an underlying dielectric layer. Bai's invention includes a barrier layer designed to "prevent physical interaction" (diffusion) of an overlying metal layer and an underlying dielectric layer. Therefore, it would have been obvious to one of ordinary skill in the art to use the diffusion barrier formation method of Elers to form the diffusion barrier of Bai.

Regarding Applicant's argument that one of ordinary skill in the art would not be motivated to use ALD to form the barrier layer of Bai, Applicant states, "However, ALD has a number of properties that make it undesirable in situations in which high conformality is not required. Foremost of these is that the monolayer by monolayer deposition by ALD is much slower than other methods that deposit multiple monolayers in each cycle, such as CVD. The high cost of an ALD process where it is not necessary would be prohibitive." Even if these statements regarding the disadvantages of the ALD process were true, it is obviously not enough of a disadvantage to persuade one of ordinary skill in the art against using ALD to deposit gate barrier layers because that is exactly what Applicant's have done in their invention. Applicant's argument that one of ordinary skill in the art would not use ALD to deposit layers in a situation in which high conformality is not required is belied by their own use of ALD to deposit a layer in

the same situation and also by the Pomarede patent which discloses using ALD to deposit a gate dielectric layer onto a flat substrate.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1839. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
November 15, 2004

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